AMENDMENTS TO THE CLAIMS

Claim 1. (Currently Amended) A method for controlling power consumption of a computer processor on a chip comprising the steps of:

determining a maximum allowable power consumption level from an operating condition of the processor,

said computer processor determining a maximum frequency which provides power not greater than the allowable power consumption level,

said computer processor determining a minimum voltage which allows operation at the maximum frequency determined, and

dynamically changing the power consumption of the processor by changing frequency and voltage, respectively, to the maximum frequency and the minimum voltage determined, wherein said dynamically changing the power consumption comprises executing instructions in said computer processor while changing voltage at which said computer processor is operated.

Claim 2. (Currently Amended) A computing device comprising:

a power supply furnishing selectable output voltages,

a clock frequency source,

a central processor including:

a processing unit for providing values indicative of operating conditions of the central processor, and

a clock frequency generator receiving a clock frequency from the clock frequency source and providing one of a plurality of selectable output clock frequencies to the processing unit; [[and]]

means for detecting the values indicative of operating conditions of the central processor and causing the power supply and clock frequency generator to furnish an output clock frequency and voltage

level for the central processor and to generate concurrently frequencies which are selected for optimum operation of a plurality of functional units of the computing device; and

means for executing instructions in said central processor while changing voltage at which said central processor is operated.

Claim 3. (Original) A computing device as claimed in Claim 2 in which the means for detecting the values indicative of operating conditions of the central processor comprises control software for determining an output clock frequency and voltage level for the central processor adapted to conserve power while maintaining an effective execution rate.

Claims 4-5. (Cancelled)

Claim 6. (Currently Amended) A method for controlling the power used by a computer comprising the steps of:

utilizing control software dedicated to a central processor to measure the operating characteristics of the central processor of the computer,

determining when the operating characteristics of the central processor are significantly different than required by the operations being conducted, and

changing the operating characteristics of the central processor to a level commensurate with the operations being conducted in which:

the step of determining when the operating characteristics of the central processor are significantly different than required by the operations being conducted comprising utilizing the control software to determine desirable voltages and frequencies for the operation of the central processor based on the measured operating characteristics, and

the step of changing the operating characteristics of the central processor to a level commensurate with the operations being conducted comprises:

providing signals:

for controlling voltages furnished by a programmable power supply to the central processor,

for controlling frequencies furnished by the central processor to the central processor, and

providing signals for controlling frequencies furnished by the central processor to other functional units of the computer; and

executing instructions in said central processor while changing voltage at which said central processor is operated.

Claim 7. (Cancelled)

Claim 8. (Currently Amended) A computer comprising:

a power supply furnishing selectable output voltages,

a clock frequency source,

a bus,

system memory,

a central processor including:

a processing unit for providing values indicative of operating conditions of the central processor, and

a clock frequency generator receiving a clock frequency from the clock frequency source and providing a plurality of selectable output clock frequencies to the processing unit; and

means for detecting the values indicative of operating conditions of the central processor and causing the power supply and clock frequency generator to furnish an output clock frequency and voltage level for the central processor and to generate concurrently

frequencies which are selected for optimum operation of a plurality of functional units of the computing device including system memory, wherein the means for detecting the values indicative of operating conditions of the central processor is further for causing execution of instructions in said central processor while changing voltage at which said central processor is operated.

Claim 9. (Original) A computer as claimed in Claim 8 in which the means for detecting the values indicative of operating conditions of the central processor comprises control software for determining an output clock frequency and voltage level for the central processor adapted to conserve power while maintaining an effective execution rate.

Claim 10. (Previously Presented) A computing device as claimed in Claim 8 in which the means for detecting the values indicative of operating conditions of the central processor causes the clock frequency generator to generate frequencies with are selected for optimum operation of system memory.

Claim 11. (Previously Presented) A computing device as claimed in Claim 8 in which the means for detecting the values indicative of operating conditions of the central processor causes the clock frequency generator to generate frequencies which are selected for optimum operation of the bus.

Claim 12-15. (Cancelled)

Claim 16. (Previously Presented) A method of controlling a computer processor, comprising:

monitoring operating conditions internal to said computer processor;

determining a frequency and a voltage at which to operate said computer processor, based on said internal operating conditions; and

implementing the determined frequency and voltage, wherein said implementing comprises:

executing instructions in said computer processor while changing voltage at which said computer processor is operated.

Claim 17-19. (Cancelled)

Claim 20. (Currently Amended) A method of controlling a computer processor, comprising:

monitoring idle time of said computer processor;

said computer processor determining a frequency and a voltage at which to operate said computer processor, based on said idle time; and

implementing the determined frequency and voltage, wherein said implementing comprises executing instructions in said computer processor while changing voltage at which said computer processor is operated.

Claim 21. (Previously Presented) The method of Claim 20, wherein said implementing comprises:

lowering frequency at which said computer processor is operated prior to lowering voltage at which said computer processor is operated.

Claim 22. (Previously Presented) The method of Claim 21, wherein said implementing further comprises:

increasing voltage at which said computer processor is operated prior to increasing frequency at which said computer processor is operated.

Claim 23. (Previously Presented) The method of Claim 20, wherein said implementing comprises:

increasing voltage at which said computer processor is operated prior to increasing frequency at which said computer processor is operated.

Claim 24. (Previously Presented) The method of Claim 20, wherein said monitoring idle time comprises monitoring internal data of said computer processor.

Claim 25. (Currently Amended) The method of Claim 20, wherein said implementing comprises:

executing instructions in said computer processor while lowering ~~changing~~ voltage at which said computer processor is operated.

Claim 26. (Previously Presented) The method of Claim 21, wherein said implementing further comprises:

executing instructions in said computer processor while lowering voltage at which said computer processor is operated.

Claim 27-28 (Cancelled).

Claim 29. (Currently Amended) A method of controlling a computer processor, comprising:

monitoring a state of said computer processor;

said computer processor determining a frequency and a voltage at which to operate said computer processor, based on said state; and

implementing the determined frequency and voltage, wherein said implementing comprises executing instructions in said computer processor while changing voltage at which said computer processor is operated.

Claim 30. (Previously Presented) The method of Claim 29, wherein said state comprises a sleep state.

Claim 31. (Previously Presented) The method of Claim 30, wherein said monitoring further comprises monitoring a halt state of said computer processor.

Claim 32. (Previously Presented) The method of Claim 29, wherein said state comprises a halt state.

Claim 33. (Previously Presented) The method of Claim 29, wherein said implementing comprises:

lowering frequency at which said computer processor is operated prior to lowering voltage at which said computer processor is operated.

Claim 34. (Previously Presented) The method of Claim 33, wherein said implementing further comprises:

increasing voltage at which said computer processor is operated prior to increasing frequency at which said computer processor is operated.

Claim 35. (Previously Presented) The method of Claim 29, wherein said implementing comprises:

increasing voltage at which said computer processor is operated prior to increasing frequency at which said computer processor is operated.

Claim 36. (Currently Amended) The method of Claim 29, wherein said implementing comprises:

executing instructions in said computer processor while lowering ~~changing~~ voltage at which said computer processor is operated.

Claim 37. (Previously Presented) The method of Claim 33, wherein said implementing further comprises:

executing instructions in said computer processor while lowering voltage at which said computer processor is operated.

Claims 38-47. (Cancelled)

Claim 48. (Currently Amended) A method of managing power consumption comprising:

monitoring internal conditions of a computer processor;

based on said internal conditions, determining an allowable power consumption level;

a computer processor determining a voltage-frequency pair for said allowable power consumption level; and

dynamically changing power consumption of the computer processor by implementing said voltage-frequency pair, wherein said dynamically changing power consumption comprises changing voltage at which said computer processor is operated while executing instructions in said computer processor.

Claim 49. (Previously Presented) The method of Claim 48, wherein said dynamically changing power consumption comprises:

lowering frequency at which said computer processor is operated prior to lowering voltage at which said computer processor is operated.

Claim 50. (Previously Presented) The method of Claim 49, wherein said dynamically changing power consumption further comprises:

increasing voltage at which said computer processor is operated prior to increasing frequency at which said computer processor is operated.

Claim 51. (Previously Presented) The method of Claim 48, wherein said dynamically changing power consumption comprises:

increasing voltage at which said computer processor is operated prior to increasing frequency at which said computer processor is operated.

Claim 52. (Cancelled)

Claim 53. (Previously Presented) The method of Claim 49, wherein said implementing further comprises:

executing instructions in said computer processor while lowering voltage at which said computer processor is operated.

Claims 54-55. (Cancelled)

Claim 56. (Previously Presented) The method of Claim 48, wherein said monitoring comprises monitoring a state of said computer processor.

Claim 57. (Previously Presented) The method of Claim 56, wherein said state comprises a halt state.

Claim 58. (Previously Presented) The method of Claim 56, wherein said state comprises a sleep state.

Claim 59. (Previously Presented) The method of Claim 58, wherein said monitoring further comprises monitoring a halt state of said computer processor.

Claim 60. (Previously Presented) The method of Claim 48, wherein said monitoring comprises monitoring a temperature.

Claim 61. (Previously Presented) The method of Claim 60, wherein said monitoring further comprises monitoring a state of said computer processor.

Claim 62. (Previously Presented) The method of Claim 61, wherein said state comprises a halt state.

Claim 63. (Previously Presented) The method of Claim 61, wherein said state comprises a sleep state.

Claim 64. (Previously Presented) The method of Claim 63, wherein said monitoring further comprises monitoring a halt state of said computer processor.

Claim 65. (Previously Presented) The method of Claim 48, wherein said determining a voltage-frequency pair comprises accessing a table of pre-determined voltage-frequency pairs.

Claim 66. (Previously Presented) The method of Claim 48, wherein said determining a voltage-frequency pair comprises calculating a voltage-frequency pair.

Claims 67-75. (Cancelled)

Claim 76. (Currently Amended) A computing device comprising:

a power supply furnishing selectable output voltages;

a clock frequency source; and

a central processor comprising:

a clock frequency generator receiving a clock frequency from the clock frequency source; and

a processing unit operable to provide values indicative of operating conditions of the central processor and to cause the power supply and the clock frequency generator to furnish a voltage level and an output clock frequency for the central processor, wherein said processing unit is further operable to cause the power supply to cause voltage furnished to the central processor to change while the central processor is executing instructions.

Claim 77. (Previously Presented) The computing device of Claim 76, wherein:

said clock frequency generator is operable to provide one of a plurality of selectable output clock frequencies to the processing unit.

Claim 78. (Previously Presented) The computing device of Claim 77, wherein:

said clock frequency generator is further operable to concurrently generate frequencies for a plurality of functional units of the computing device.

Claim 79. (Previously Presented) The computing device of Claim 76, wherein:

said clock frequency generator is operable to concurrently generate frequencies for a plurality of functional units of the computing device.

Claim 80. (Previously Presented) The method of Claim 1, wherein said dynamically changing the power consumption comprises increasing voltage prior to increasing frequency.

Claim 81. (Previously Presented) The method of Claim 60, wherein said dynamically changing the power consumption comprises lowering frequency prior to lowering voltage.

Claim 82. (Previously Presented) The method of Claim 1, wherein said dynamically changing the power consumption comprises lowering frequency prior to lowering voltage.

Claim 83. (Currently Amended) The method of Claim 1, wherein said dynamically changing the power consumption comprises:

executing said instructions in said computer processor while lowering ~~changing~~ voltage at which said computer processor is operated.

Claim 84. (Previously Presented) The method of Claim 82, wherein dynamically changing the power consumption further comprises:

executing instructions in said computer processor while lowering voltage at which said computer processor is operated.

Claims 85-86. (Cancelled)

Claim 87. (Previously Presented) The method of Claim 1, wherein said dynamically changing the power consumption comprises concurrently generating a plurality of frequencies.

Claim 88. (Previously Presented) The method of Claim 1, wherein said operating condition of the processor is internal to the processor.

Claims 89-92. (Cancelled)

Claim 93. (Currently Amended) The method of Claim [[12]] 16, wherein said monitoring comprises said computer processor monitoring operating conditions internal to said computer processor.

Claim 94. (New) The method of Claim 16, wherein said implementing comprises lowering frequency at which said computer processor is operated

Claim 95. (New) The method of Claim 94, wherein said changing voltage comprises lowering voltage at which said computer processor is operated.

Claim 96. (New) The method of Claim 95, wherein said lowering voltage occurs after said lowering frequency.

Claim 97. (New) The method of Claim 16, wherein said implementing comprises:

increasing frequency at which said computer processor is operated.

Claim 98. (New) The method of Claim 97, wherein said changing voltage comprises increasing voltage at which said computer processor is operated.

Claim 99. (New) The method of Claim 98, wherein said increasing voltage occurs prior to said increasing frequency.